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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,592	RYCHLIK ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 20-38 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: RCE and Amendment as received on 5/16/2005.

Specification

3. The amended abstract filed on May 16, 2005, is objected to because it does not appear on a separate sheet. "A replacement or new abstract must be submitted on a separate sheet, 37 CFR 1.72." See http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/officeflyer.pdf and note section B of the Office Flyer.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20-24, 27-31, and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Redford, U.S. Patent No. 5,870,581 (as applied in the previous Office Action), in view of Intel, "IA-64 Application Developer's Architecture Guide," May 1999 (as applied in the previous Office Action and herein referred to as Intel), and further in view of Hennessy and

Patterson, "Computer Architecture - A Quantitative Approach, 2nd Edition," 1996 (as partially applied in the previous Office Action and herein referred to as Hennessy).

6. Referring to claim 20, Redford has taught an apparatus comprising:

a) a first register file of a plurality of register files to store values. See Fig.3, component 22.

b) a second register file of said plurality of register files to receive results from execution of a first instruction when said first register file is busy. See Fig.3, components 62 and 64 (note that the two temporary registers make up a temporary register file). Also, from Fig.4, if the first register file cannot accept data (busy) from a writing instruction (step 86), then the data is written to the temporary register file (step 92).

c) Redford has not taught that the values stored by the registers are predicate values. However, Intel has taught the concept of registers holding predicate values. See page 3-4, section 3.1.4. By implementing predicates, conditional execution may be achieved, thereby eliminating branch instructions and associated misprediction penalties, and resulting in larger basic blocks. See page 2-4, section 2.6.3. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Redford to include predicate registers. One would've been motivated to do so because Redford's teachings would also apply to predicate registers. More specifically, predicate registers are read from and written to just like any other normal registers, such as the ones taught by Redford. Therefore, if predicate register files were to be busy, additional predicate values may be stored in a second register file.

d) Redford has also not taught that the first instruction is an instruction which writes to multiple predicate registers. However, if predicate registers are added to Redford, as taught above, then there must be instructions which write to the predicate registers. Intel has taught a "Move

Predicates" instruction and also a "Compare" instruction. See pages 7-19 and 7-127. Both of these instructions will write to multiple predicate registers. Clearly, this is beneficial as multiple predicates may be written at once as opposed to one at a time. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Redford to include an instruction which writes to multiple predicate registers.

e) Finally, Redford has not taught assigning a register file for register renaming in an out-of-order processor. However, Hennessy has taught such a concept. First, see page 241 ("Dynamic Scheduling: The Idea") and note that out-of-order processors allow non-dependent instructions to continue executing even if a prior instruction is stalled due to a dependency. This prevents functional units from sitting idle and ultimately increases throughput. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Redford to be an out-of-order processor. Furthermore, Hennessy discloses that dynamic scheduling (out-of-order scheduling) may be performed by using a scoreboard (page 242, "Dynamic Scheduling with a Scoreboard") and a scoreboard, in turn, may be combined with register renaming (page 251, 2nd to last paragraph). As is known in the art, register renaming is a technique used to avoid unnecessary serialization of program operations imposed by the reuse of registers by those operations. More specifically, register renaming dynamically eliminates name dependences in order to avoid WAR and WAW hazards (see the middle of page 251 of Hennessy), which would decrease stalling in the processor. As a result, in order to increase efficiency of the processor, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Redford to include register renaming.

7. Referring to claim 21, Redford in view of Intel and further in view of Hennessy has taught an apparatus as described in claim 20. Redford in view of Intel and further in view of Hennessy has further taught a select register to indicate which of said plurality of register files is being written to by execution of a second instruction that writes to multiple predicate registers. Clearly, in order for the system to determine which file is written to, a value must be checked (in this case, it would be the busy value which is checked at step 86 of Redford). This value is inherently stored somewhere and this storage is the select register.

8. Referring to claim 22, Redford in view of Intel and further in view of Hennessy has taught an apparatus as described in claim 21. Redford has further taught that the select register includes a pointer to said which of said plurality of register files. Since the select register holds a value which tells the system where to store the data (actual register file or temporary register file), then it indeed stores a pointer to the storage file.

9. Referring to claim 23, Redford in view of Intel and further in view of Hennessy has taught an apparatus as described in claim 20. Redford in view of Intel has not explicitly taught that said first register file indicates that it is busy with a scoreboard. However, Hennessy has taught the idea of a scoreboard for tracking if a register file is busy. See page 247, and note that fields Rj and Rk of the scoreboard track if a register, and hence, its associated register file, are busy. As discussed on page 242, a scoreboard is useful for allowing out-of-order execution, which is a technique that has advantages known in the art. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Redford in view of Intel to have a scoreboard for tracking business of register files.

10. Referring to claim 24, Redford in view of Intel and further in view of Hennessy has taught an apparatus as described in claim 23. Redford in view of Intel and further in view of Hennessy has further taught that said apparatus stalls execution of a third instruction that writes to at most two predicate registers (Intel's compare instruction) when said scoreboard indicates destination registers of said third instruction are busy. See Fig.4, steps 86, 92, and 94. Note that if a register file is busy (step 86), then the system determines if the temporary register file is busy (step 90). If it is not busy, then the instruction may continue and write the data to the temporary register file (step 92). However, if the temporary register file is busy, then the instruction may not proceed (stall).

11. Referring to claim 27, the apparatus of claim 20 performs the method of claim 27. Consequently, claim 27 is rejected for the same reasons set forth in the rejection of claim 20.

12. Referring to claim 28, Redford in view of Intel and further in view of Hennessy has taught a method as described in claim 27. Furthermore, the apparatus of claim 21 performs the method of claim 28. Consequently, claim 28 is rejected for the same reasons set forth in the rejection of claim 21.

13. Referring to claim 29, Redford in view of Intel and further in view of Hennessy has taught a method as described in claim 28. Furthermore, the apparatus of claim 22 performs the method of claim 29. Consequently, claim 29 is rejected for the same reasons set forth in the rejection of claim 22.

14. Referring to claim 30, Redford in view of Intel and further in view of Hennessy has taught a method as described in claim 27. Furthermore, the apparatus of claim 23 performs the

method of claim 30. Consequently, claim 30 is rejected for the same reasons set forth in the rejection of claim 23.

15. Referring to claim 31, Redford in view of Intel and further in view of Hennessy has taught a method as described in claim 30. Furthermore, the apparatus of claim 24 performs the method of claim 31. Consequently, claim 31 is rejected for the same reasons set forth in the rejection of claim 24.

16. Referring to claim 34, the system of claim 34 includes the apparatus of claim 20. Consequently, the first portion (lines 1-6) of claim 34 is rejected for the same reasons set forth in the rejection of claim 20. In addition, Redford has taught:

a) interface logic to couple said processor to input/output devices. See Fig.1, component 2.

b) Redford has not taught a disk drive coupled to said processor via said interface logic. However, Official Notice is taken that disk drives are well known and expected in the art. A disk drive allows a processor to store large amounts of data in relatively cheap storage. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Redford to include a disk drive that coupled to the interface logic.

17. Referring to claim 35, Redford in view of Intel and further in view of Hennessy has taught a system as described in claim 34. Furthermore, the apparatus of claim 21 includes the same specifics as the system of claim 35. Consequently, claim 35 is rejected for the same reasons set forth in the rejection of claim 21.

18. Referring to claim 36, Redford in view of Intel and further in view of Hennessy has taught a system as described in claim 34. Furthermore, the system of claim 36 includes the same

specifics as the apparatus of claim 23. Consequently, claim 36 is rejected for the same reasons set forth in the rejection of claim 23.

19. Referring to claim 37, Redford in view of Intel and further in view of Hennessy has taught a system as described in claim 36. Furthermore, the system of claim 37 includes the same specifics as the apparatus of claim 24. Consequently, claim 37 is rejected for the same reasons set forth in the rejection of claim 24.

20. Claims 25-26, 32-33, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Redford in view of Intel in view of Hennessy, as applied above, and further in view of Nojiri, U.S. Patent No. 5,179,685 (as applied in the previous Office Action).

21. Referring to claim 25, Redford in view of Intel in view of Hennessy has taught an apparatus as described in claim 20. Redford in view of Intel in view of Hennessy has not taught a free file list to point to the next in order of said plurality of register files that is not busy. However, Nojiri has taught such a concept. See Fig.1, components 4, and column 3, lines 21-23. From column 3, lines 5-42, it can be seen that this is useful so that the required amount of register files may be allocated to a particular task, and it is easy to track free and busy files. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Redford in view of Intel to include a free file list.

22. Referring to claim 26, Redford in view of Intel in view of Hennessy and further in view of Nojiri has taught an apparatus as described in claim 25. Nojiri has further taught that the free file list indicates which of said plurality of register files are to be de-allocated. See column 3,

lines 26-29. Note that is a register file is no longer needed, then it is added to the free file list, where it is deallocated and eventually reallocated to another task which can use it.

23. Referring to claim 32, Redford in view of Intel and further in view of Hennessy has taught a method as described in claim 27. Furthermore, the apparatus of claim 25 performs the method of claim 32. Consequently, claim 32 is rejected for the same reasons set forth in the rejection of claim 25.

24. Referring to claim 33, Redford in view of Intel in view of Hennessy and further in view of Nojiri has taught a method as described in claim 32. Furthermore, the apparatus of claim 26 performs the method of claim 33. Consequently, claim 33 is rejected for the same reasons set forth in the rejection of claim 26. Also, since a first register file is already allocated and a next register file has not yet been allocated, then the pointing indicates that the first register file is earlier in order (allocated earlier).

25. Referring to claim 38, Redford in view of Intel and further in view of Hennessy has taught a system as described in claim 34. Furthermore, the system of claim 38 includes the same specifics as the apparatus of claim 25. Consequently, claim 38 is rejected for the same reasons set forth in the rejection of claim 25.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
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July 21, 2005

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